ABSTRACT OF THE DISCLOSURE

Disclosed is a clock and data recovery circuit for improving the tracking speed against fluctuations or variations in a received data signal, and the clock quality, and for allowing automatic adjustment to an optimum phase of discrimination. The clock and data recovery circuit includes a first feedback loop 204 made up by a phase detector circuit 209 receiving the clock from a VCO 203 and a received data signal to detect the phase difference between them, an integrator circuit 210, and the VCO 203, and a second feedback loop 207 made up by a discriminator 205, supplied with a received data signal 201, a phase detector circuit 211 supplied with an output of the discriminator 205, a phase detector circuit 211 supplied with an output of the discriminator 205 and with the received data signal 201 to detect the phase difference between them, an integrator circuit 212, and a phase shifter 208 receiving the clock output from the discriminator 203 to shift the phase of the clock in accordance with an integrated output of the integrator circuit 212 to output the resulting clock.